OBLON, SPIVAK, ET AL
DOCKET #:205368US2
INV:Harutaka GOTO
SHEET 1 OF 13

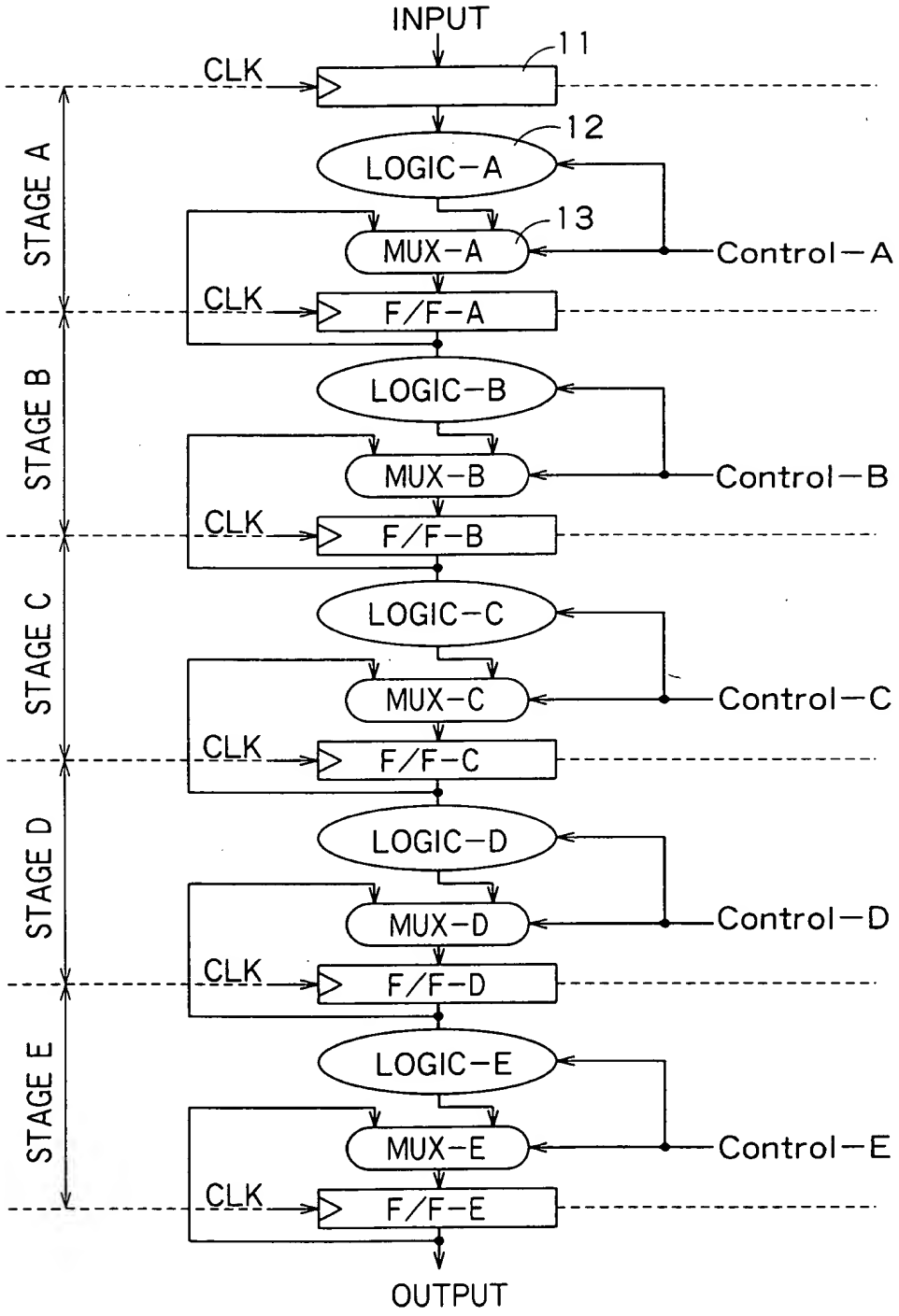

FIG. 1

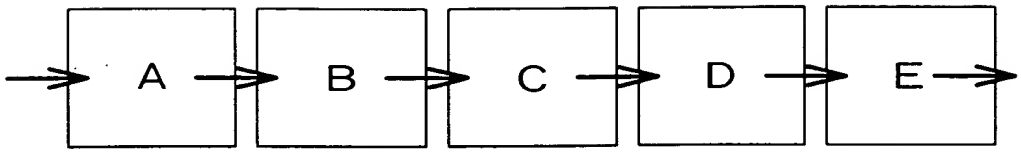
A
B
C
D
E

FIG. 2

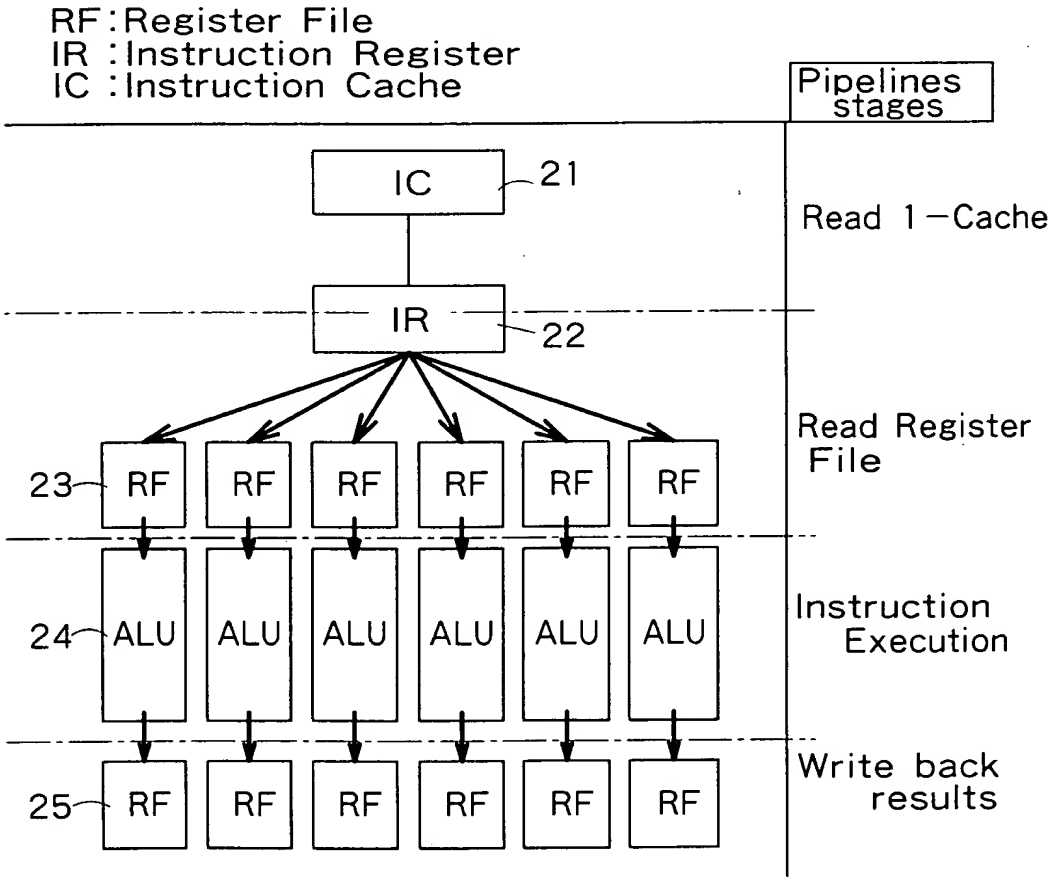
RF:Register File
IR :Instruction Register
IC :Instruction Cache
Pipelines stages
IC
21
Read 1−Cache
IR
22
Read Register File
23
RF
24
ALU
Instruction Execution
25
Write back results

FIG. 3

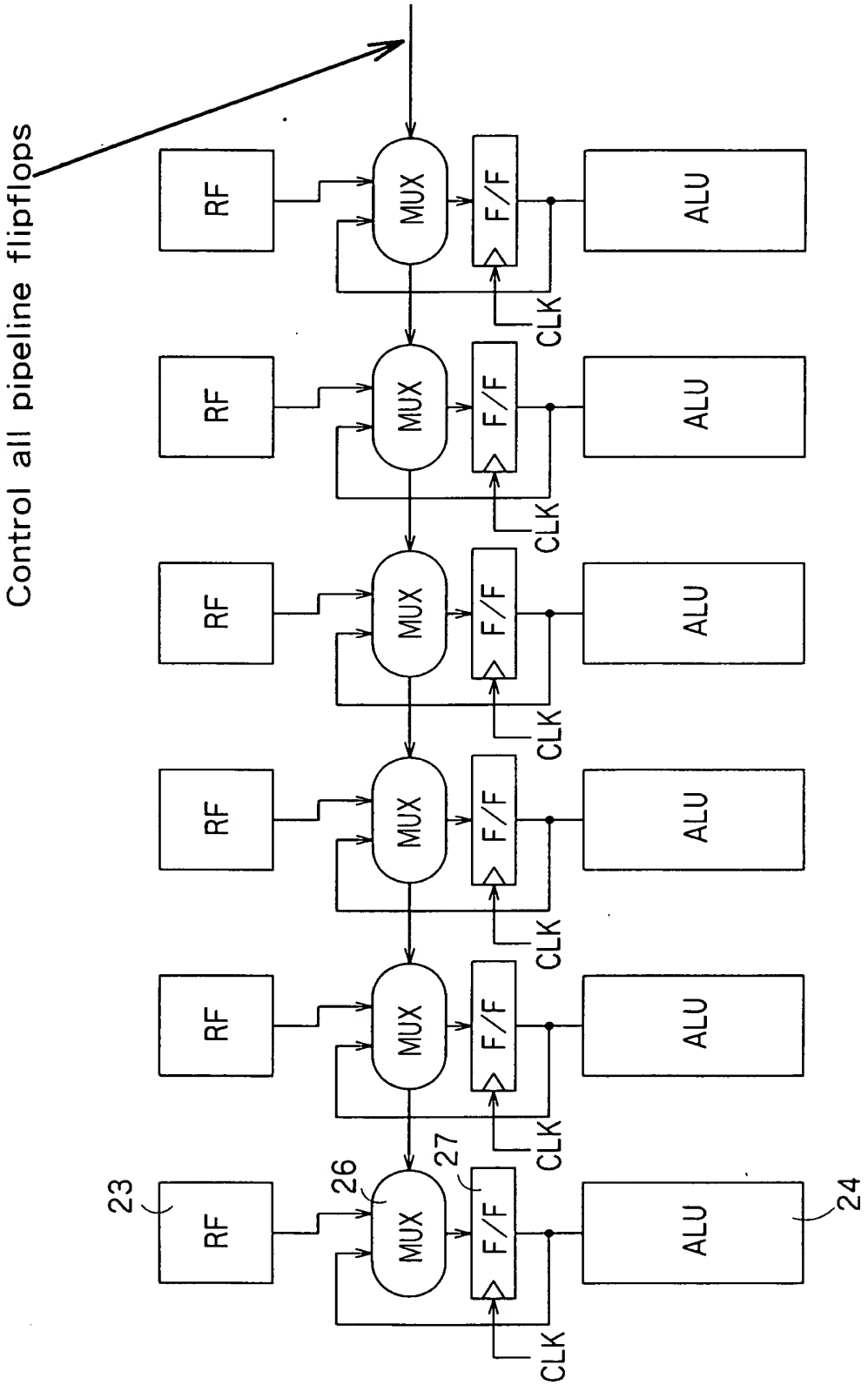

FIG. 4

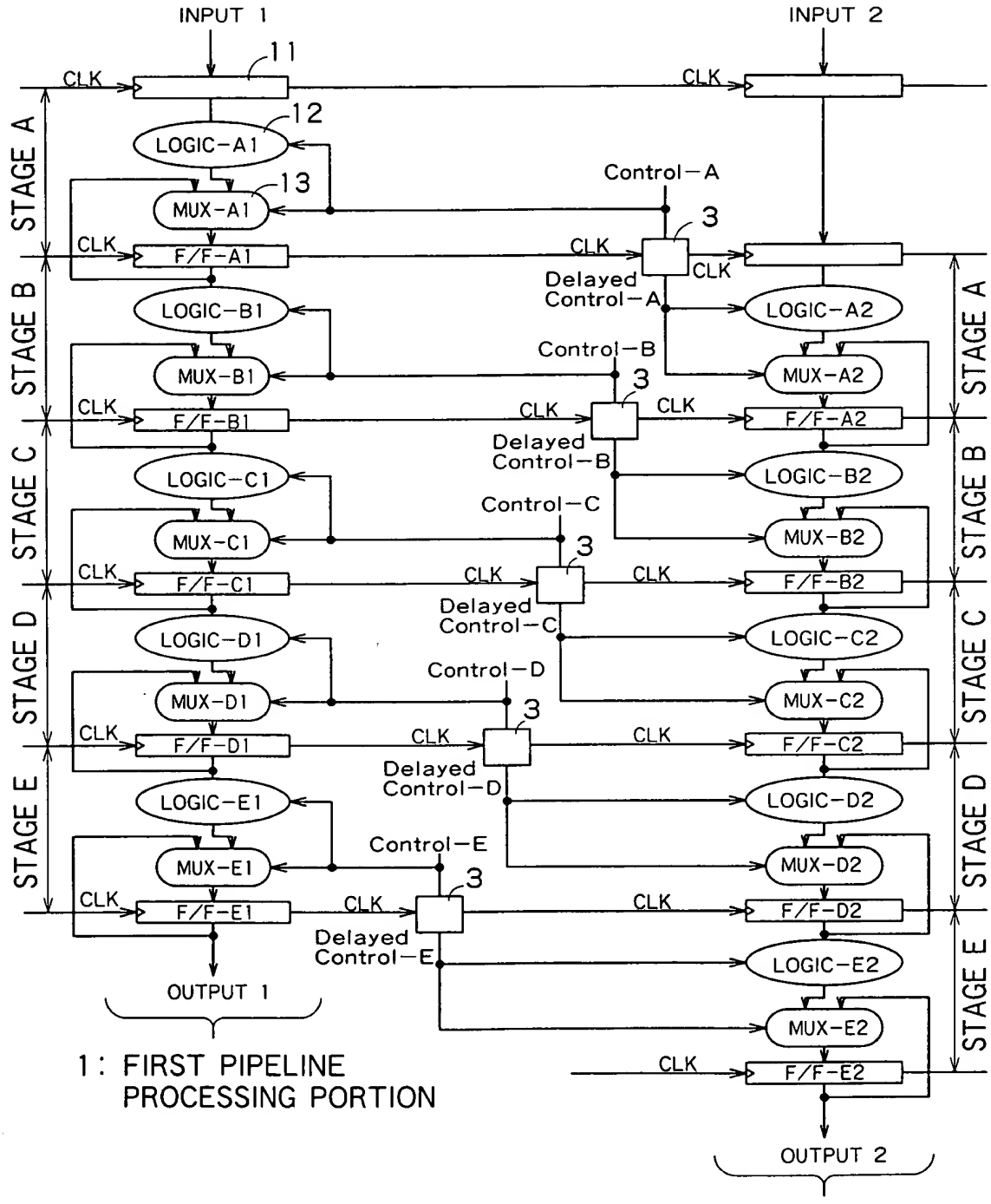
INPUT 1
INPUT 2
CLK
11
12
LOGIC-A1
13
MUX-A1
F/F-A1
LOGIC-B1
MUX-B1
F/F-B1
LOGIC-C1
MUX-C1
F/F-C1
LOGIC-D1
MUX-D1
F/F-D1
LOGIC-E1
MUX-E1
F/F-E1
OUTPUT 1
STAGE A
STAGE B
STAGE C
STAGE D
STAGE E
Control-A
Control-B
Control-C
Control-D
Control-E
3
Delayed Control-A
Delayed Control-B
Delayed Control-C
Delayed Control-D
Delayed Control-E
LOGIC-A2
MUX-A2
F/F-A2
LOGIC-B2
MUX-B2
F/F-B2
LOGIC-C2
MUX-C2
F/F-C2
LOGIC-D2
MUX-D2
F/F-D2
LOGIC-E2
MUX-E2
F/F-E2
OUTPUT 2
1: FIRST PIPELINE PROCESSING PORTION
2: SECOND PIPELINE PROCESSING PORTION

FIG. 5

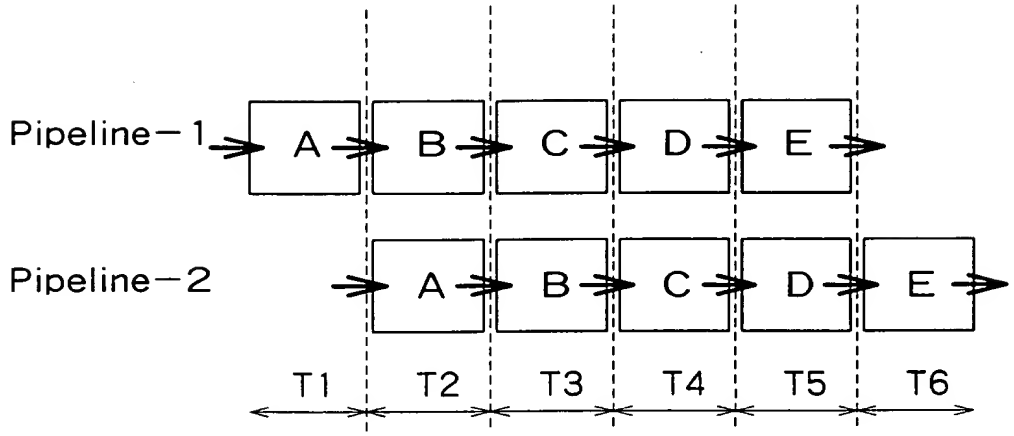
Pipeline−1
A
B
C
D
E
Pipeline−2
A
B
C
D
E
T1
T2
T3
T4
T5
T6

FIG. 6A

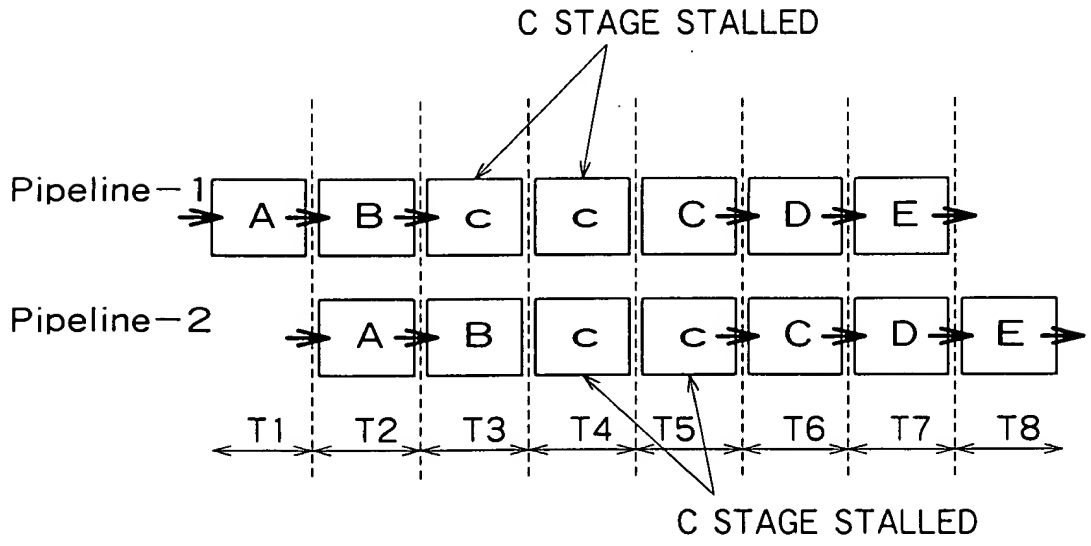
C STAGE STALLED
Pipeline−1
A
B
c
c
C
D
E
Pipeline−2
A
B
c
c
C
D
E
T1
T2
T3
T4
T5
T6
T7
T8
C STAGE STALLED

FIG. 6B

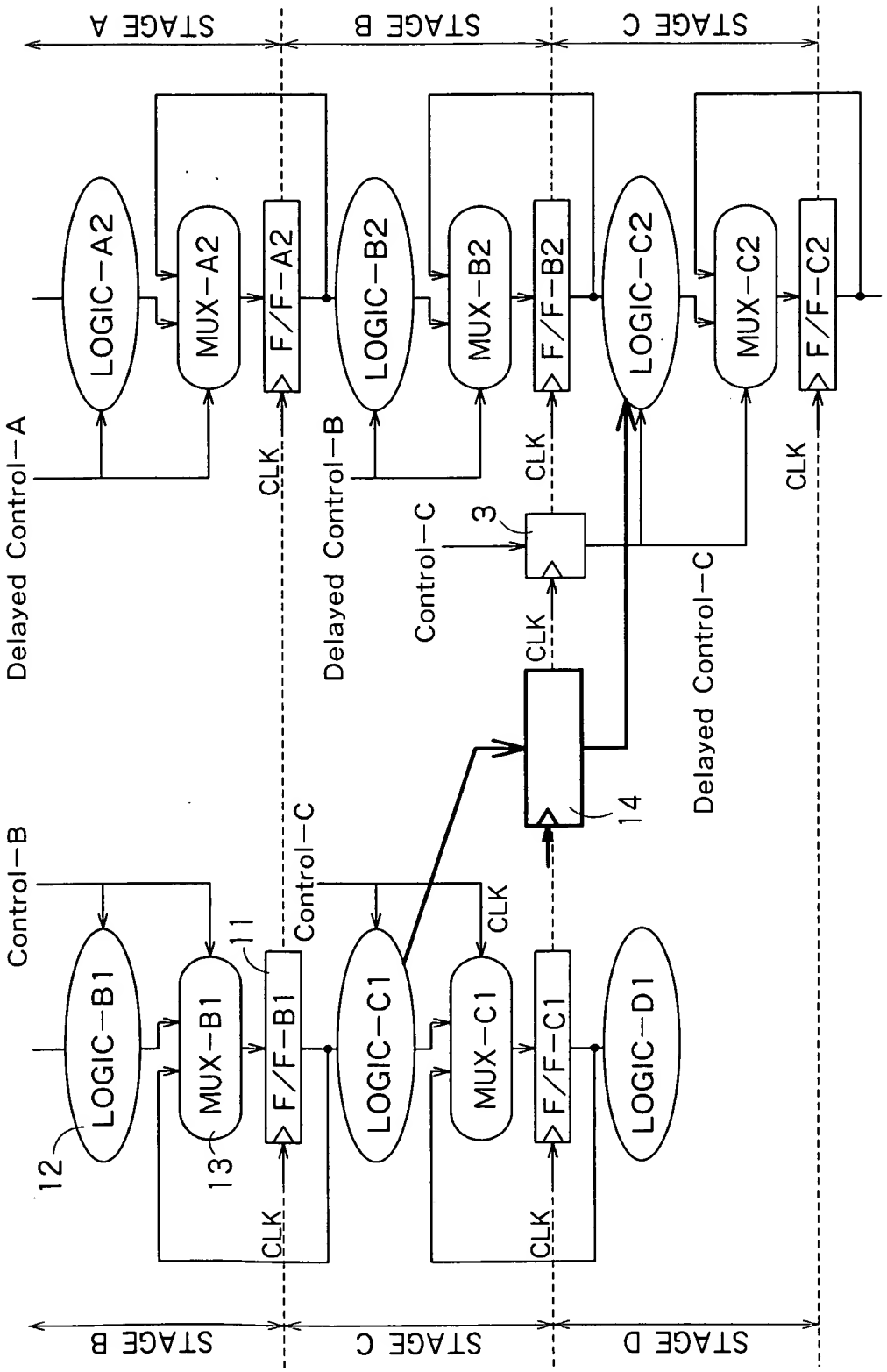
STAGE A
STAGE B
STAGE C
STAGE B
STAGE C
STAGE D
LOGIC-A2
MUX-A2
F/F-A2
LOGIC-B2
MUX-B2
F/F-B2
LOGIC-C2
MUX-C2
F/F-C2
Delayed Control-A
Delayed Control-B
Control-C
Delayed Control-C
CLK
3
14
Control-B
Control-C
11
12
13
LOGIC-B1
MUX-B1
F/F-B1
LOGIC-C1
MUX-C1
F/F-C1
LOGIC-D1

FIG. 7

7 / 13

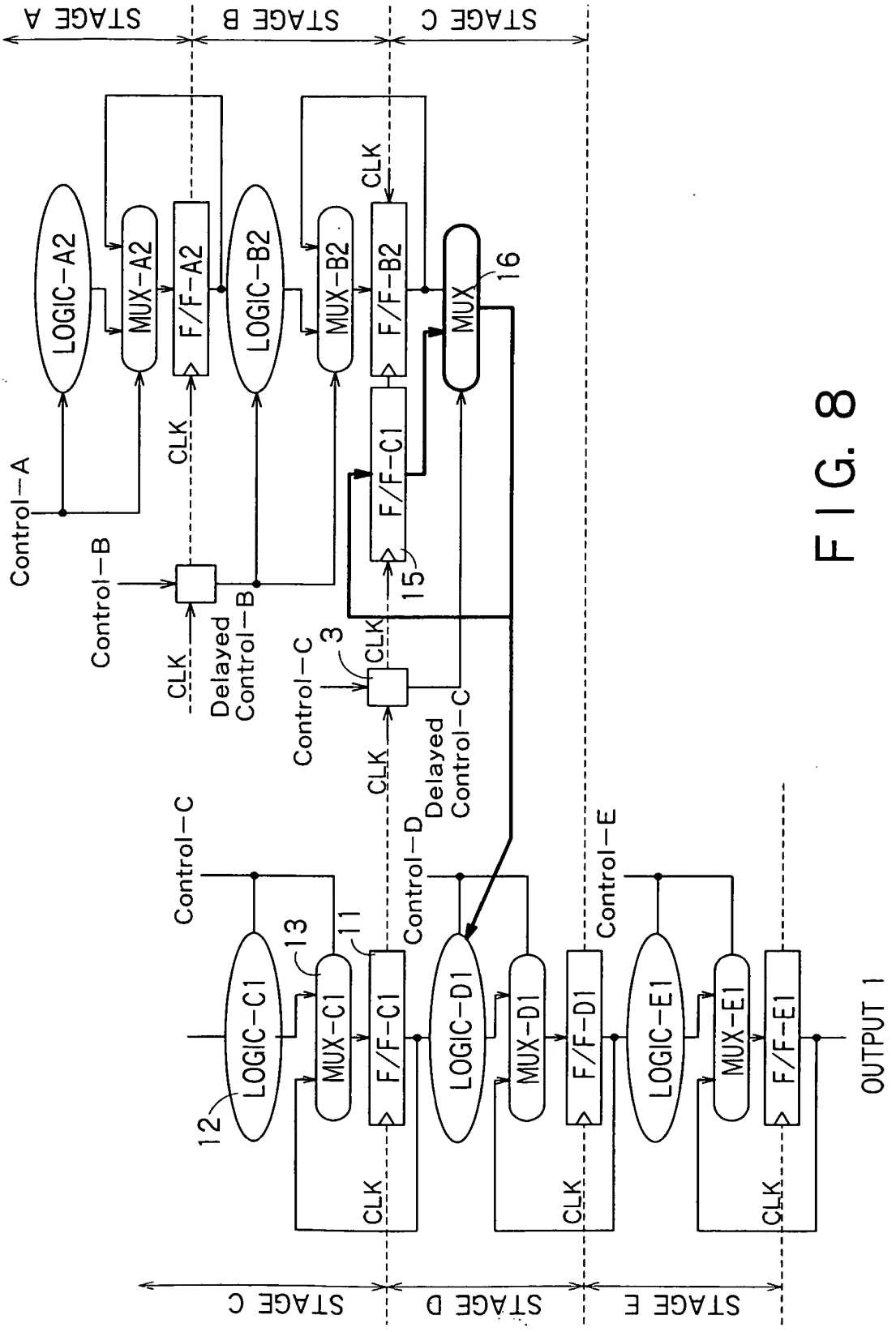
STAGE A
STAGE B
STAGE C
STAGE C
STAGE D
STAGE E
LOGIC-A2
MUX-A2
F/F-A2
LOGIC-B2
MUX-B2
F/F-B2
MUX
16
F/F-C1
15
Control-A
Control-B
CLK
Delayed Control-B
Control-C
3
Delayed Control-C
Control-D
Control-E
LOGIC-C1
MUX-C1
F/F-C1
LOGIC-D1
MUX-D1
F/F-D1
LOGIC-E1
MUX-E1
F/F-E1
12
13
11
OUTPUT 1

FIG. 8

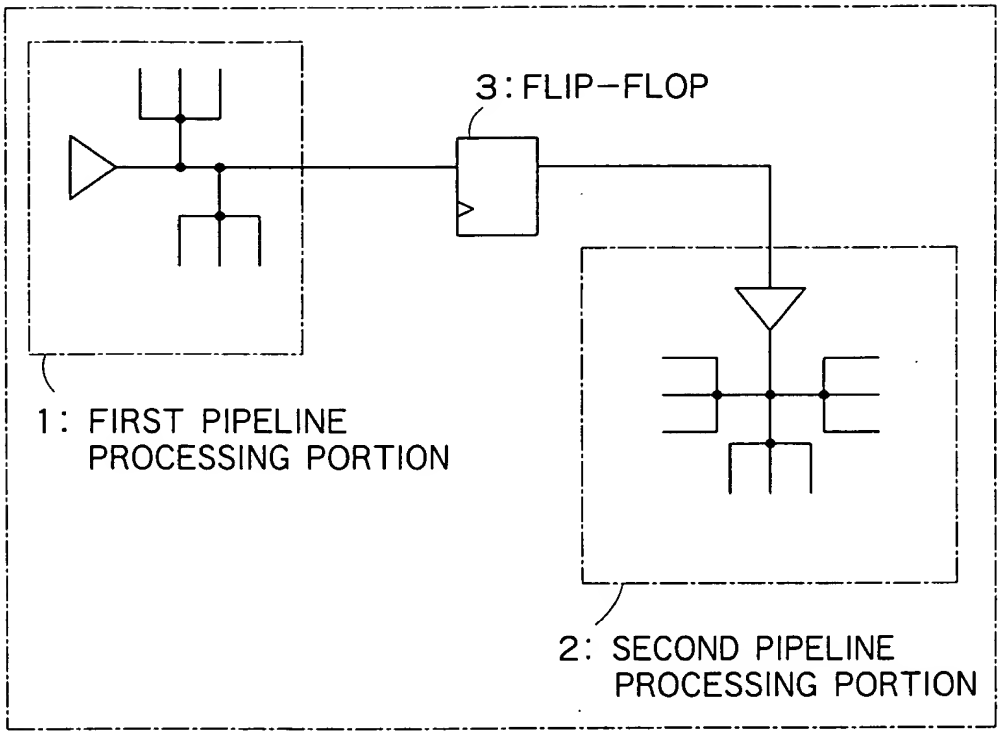
3: FLIP-FLOP
1: FIRST PIPELINE PROCESSING PORTION
2: SECOND PIPELINE PROCESSING PORTION

FIG. 9

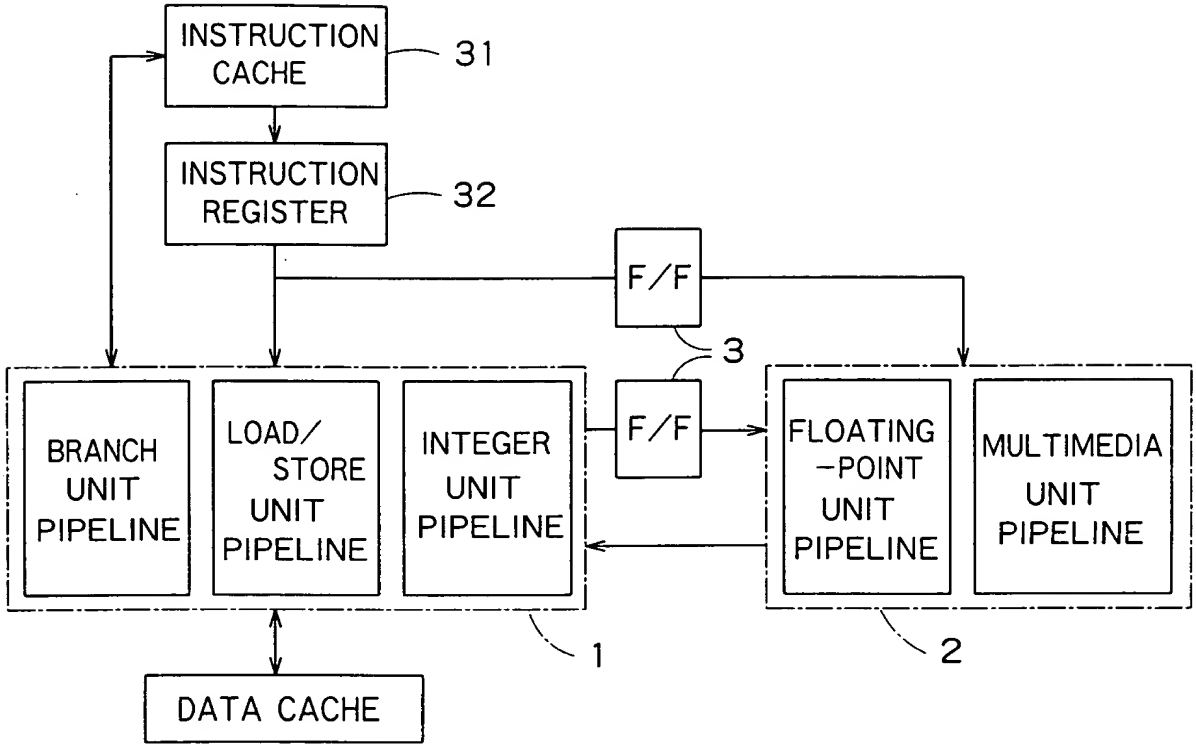
INSTRUCTION CACHE
31
INSTRUCTION REGISTER
32
F/F
3
BRANCH UNIT PIPELINE
LOAD/ STORE UNIT PIPELINE
INTEGER UNIT PIPELINE
F/F
FLOATING -POINT UNIT PIPELINE
MULTIMEDIA UNIT PIPELINE
1
2
DATA CACHE

FIG. 10

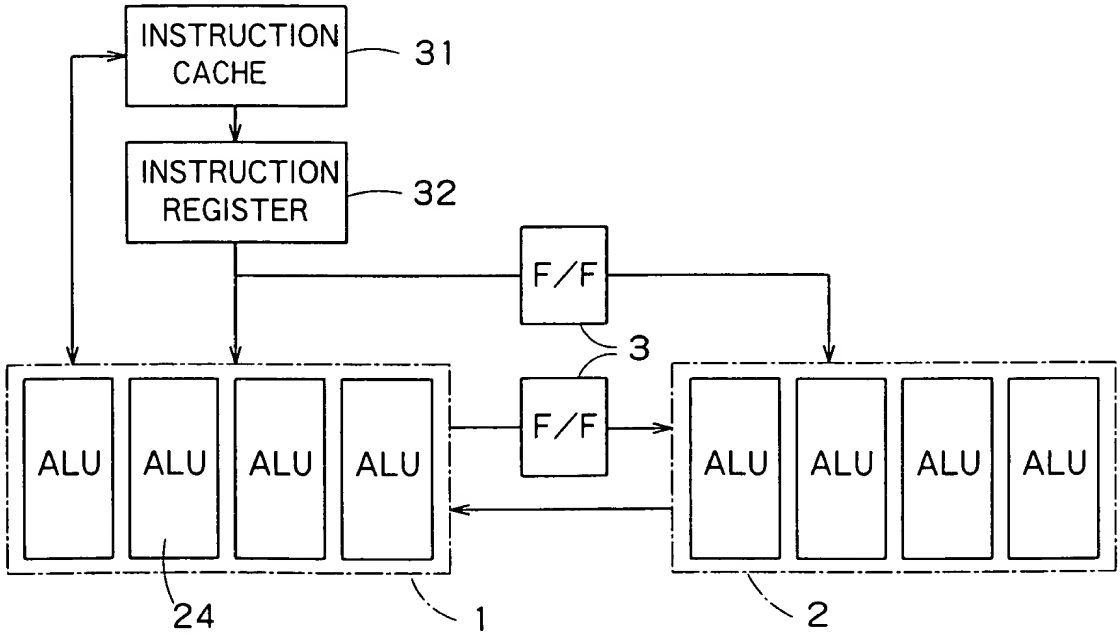
INSTRUCTION CACHE
31
INSTRUCTION REGISTER
32
F/F
3
ALU
ALU
ALU
ALU
F/F
ALU
ALU
ALU
ALU
24
1
2

FIG. 11

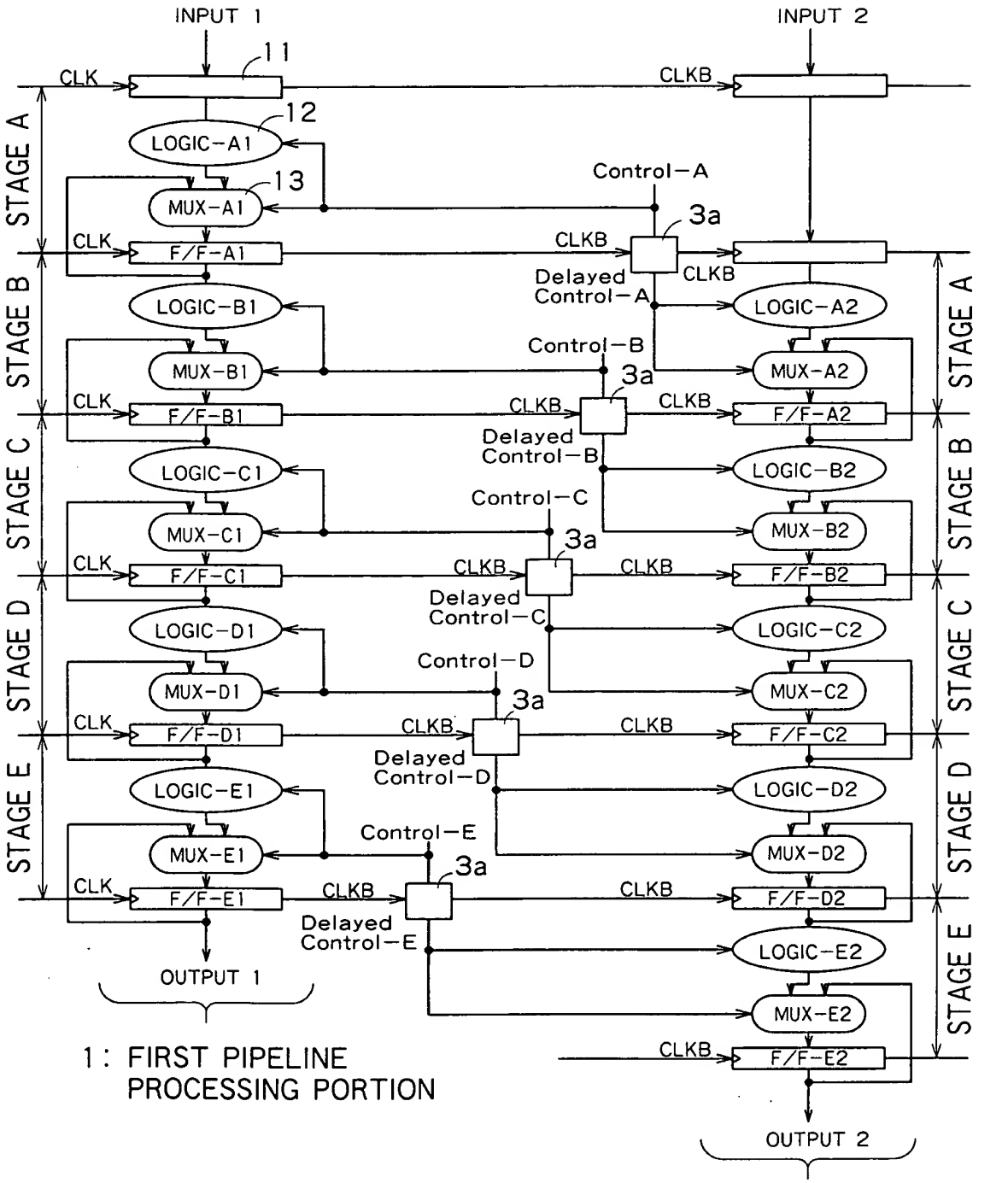
INPUT 1
INPUT 2
11
12
13
3a
CLK
CLKB
STAGE A
STAGE B
STAGE C
STAGE D
STAGE E
LOGIC-A1
MUX-A1
F/F-A1
LOGIC-B1
MUX-B1
F/F-B1
LOGIC-C1
MUX-C1
F/F-C1
LOGIC-D1
MUX-D1
F/F-D1
LOGIC-E1
MUX-E1
F/F-E1
Control-A
Control-B
Control-C
Control-D
Control-E
Delayed Control-A
Delayed Control-B
Delayed Control-C
Delayed Control-D
Delayed Control-E
LOGIC-A2
MUX-A2
F/F-A2
LOGIC-B2
MUX-B2
F/F-B2
LOGIC-C2
MUX-C2
F/F-C2
LOGIC-D2
MUX-D2
F/F-D2
LOGIC-E2
MUX-E2
F/F-E2
OUTPUT 1
OUTPUT 2
1: FIRST PIPELINE PROCESSING PORTION
2: SECOND PIPELINE PROCESSING PORTION

FIG. 12

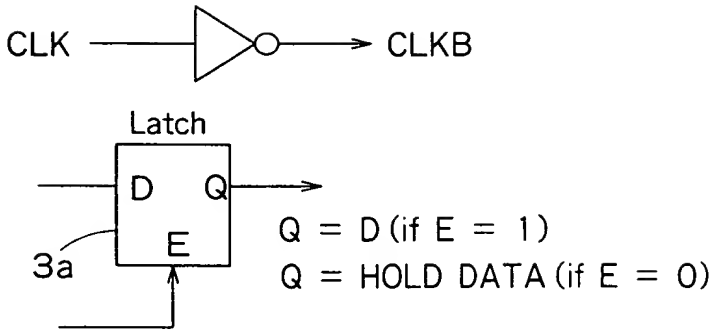

FIG. 13

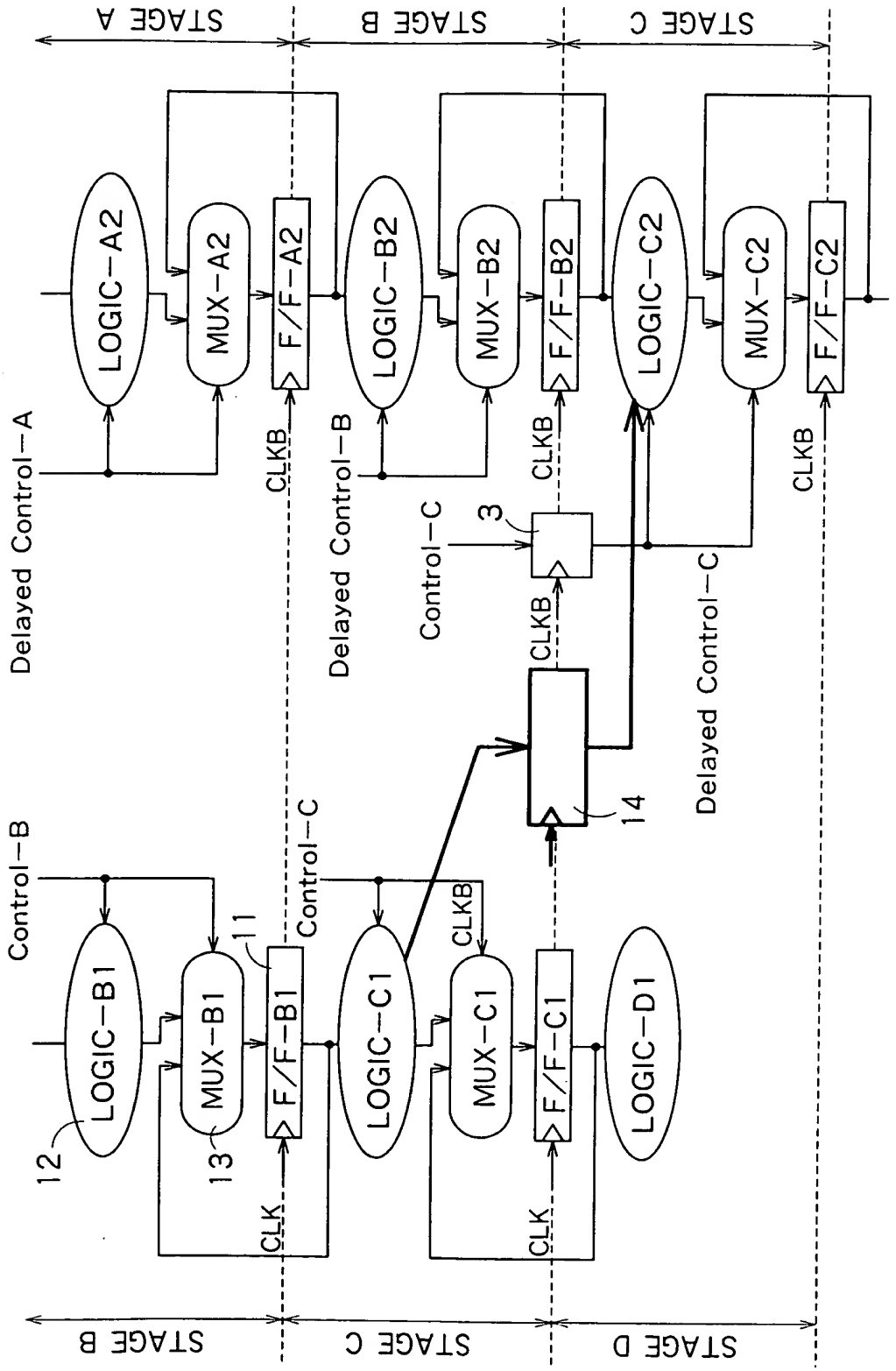
STAGE A
STAGE B
STAGE C
STAGE B
STAGE C
STAGE D
LOGIC-A2
MUX-A2
F/F-A2
LOGIC-B2
MUX-B2
F/F-B2
LOGIC-C2
MUX-C2
F/F-C2
LOGIC-B1
MUX-B1
F/F-B1
LOGIC-C1
MUX-C1
F/F-C1
LOGIC-D1
Delayed Control-A
Delayed Control-B
Control-C
Delayed Control-C
Control-B
Control-C
CLKB
CLK
3
11
12
13
14

FIG. 14

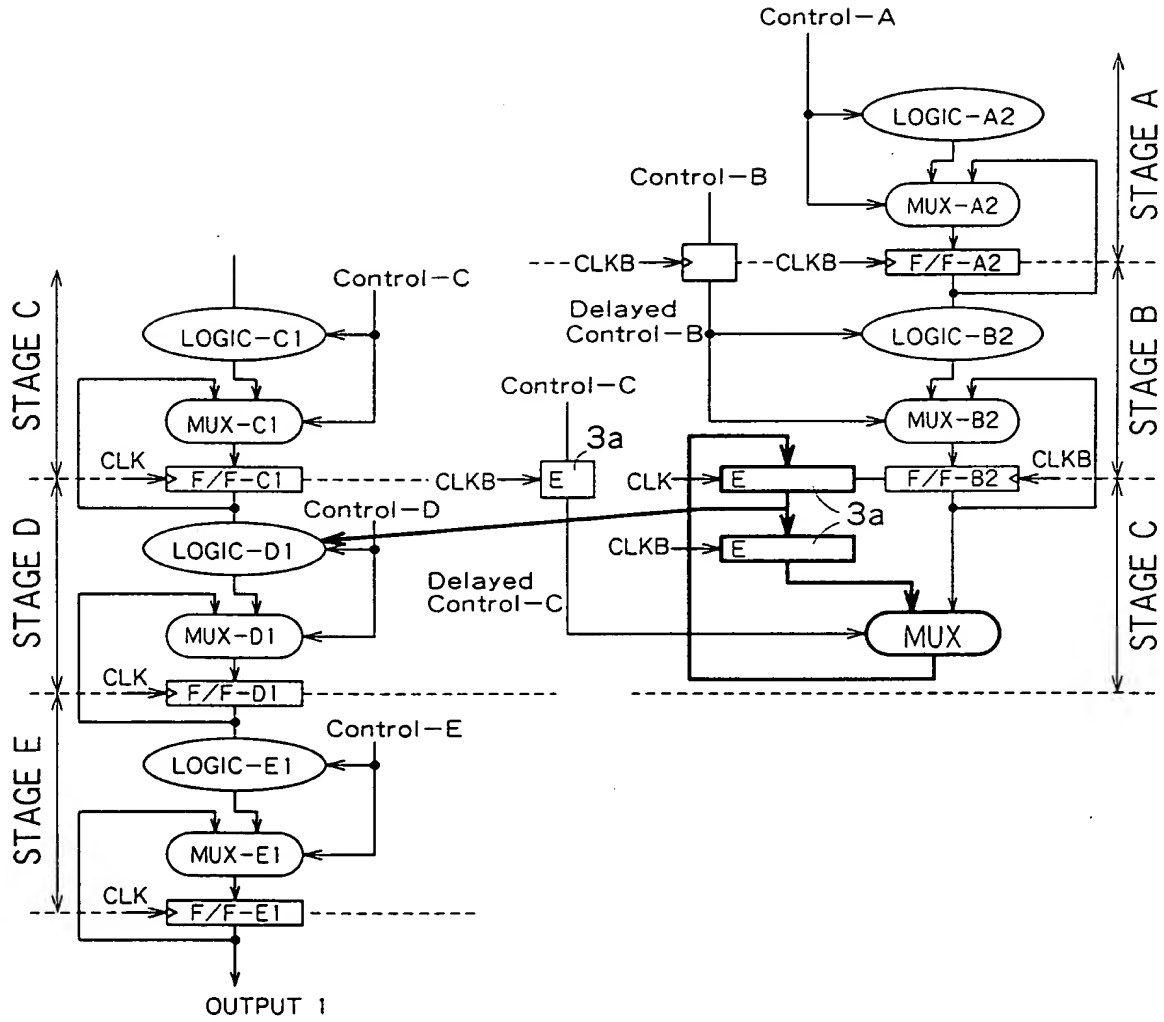
Control—A
LOGIC—A2
STAGE A
Control—B
MUX—A2
CLKB
CLKB
F/F—A2
Delayed
Control—B
LOGIC—B2
STAGE B
Control—C
MUX—B2
3a
CLK
F/F—C1
CLKB
E
CLK
E
F/F—B2
CLKB
Control—D
3a
LOGIC—D1
CLKB
E
STAGE C
Delayed
Control—C
MUX
MUX—D1
CLK
F/F—D1
Control—E
LOGIC—E1
STAGE D
MUX—E1
CLK
F/F—E1
OUTPUT 1
STAGE E

FIG. 15